



05-09-03

2813

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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	09/388,826
	Filing Date	September 1, 1999
	First Named Inventor	Weimin Li, et al.
	Group Art Unit	2813
	Examiner Name	E. Kielin
Total Number of Pages in This Submission		Attorney Docket Number MI22-1208

ENCLOSURES (check all that apply)		
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<input type="checkbox"/> Affidavits/declaration(s)	<input type="checkbox"/> Petition to Convert to a Provisional Application	<input type="checkbox"/> Status Letter
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<input checked="" type="checkbox"/> Supplemental Information Disclosure Statement	<input type="checkbox"/> Small Entity Statement	
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Firm or Individual name	D. Brent Kenady; Wells, St. John, PS
Signature	
Date	5-7-03

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EV085430309



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/388,826
Filing Date September 1, 1999
Inventor Weimin (Michael) Li et al.
Assignee Micron Technology, Inc.
Group Art Unit 2813
Examiner E. Kielin
Attorney's Docket No. MI22-1208
Title: Low k Interlevel Dielectric Layer Fabrication Methods

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References –See Attached Form PTO-1449

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the references which are listed on the attached Form PTO-1449, copies of which are attached. No admission is made regarding whether all the submitted references are prior art.

Citation of the referenced art is respectfully requested.

This Supplemental Information Disclosure Statement is being filed after the filing of the Request for Continued Examination (RCE) Application and before receipt of the first Office Action. Therefore, no fee is believed to be required. However, in the event that a fee is required for filing this Supplemental Information Disclosure Statement, please charge the fee specified under 37 C.F.R. § 1.17(p) to Deposit Account No. 23-0925. Please credit Deposit Account No. 23-0925 with any overpayment of the above fee.

Respectfully submitted,

Dated: 5-7-03

By: [Signature]
D. Brent Kenady
Reg. No. 40,045

Form PTO-1449 <div style="position: absolute; top: 0; left: 0; border: 2px solid black; border-radius: 50%; padding: 10px; transform: rotate(-45deg); transform-origin: center;"> OIPE MAY 07 2002 U.S. PATENT & TRADEMARK OFFICE </div>		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-1208		SERIAL NO. 09-388,826	
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Weimin (Michael) Li et al.			
				FILING DATE September 1, 1999		GROUP 2813	
U.S. PATENT DOCUMENTS							
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
AA	6,087,064	07/00	Lin, et al.				
AB							
AC							
AD							
AE							
AF							
AG							
AH							
AI							
AJ							
FOREIGN PATENT DOCUMENTS							
	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
AK							
AL							
AM							
AN							
AO							
AP							
AQ							
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
AR		Wolt et al., "Silicon Processing for the VLSI Era - Vol. 1 - Process Technology," Prologue, page xxiii (2 pages total).					
AS							
AT							
EXAMINER				DATE CONSIDERED			
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

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